Overview

All power supplies require some type of feedback loop to regulate the output voltage. A simplified diagram of a buck controller is shown in Figure 1 with a pulse width modulator (PWM) and an error amplifier / compensator.

For this feedback loop to be stable, negative feedback is used. This means that the output voltage (V_{OUT}) is compared to the reference voltage (V_R) and the difference ($V_R - V_{OUT}$) is amplified by the error amplifier. The output of the error amplifier is called the error voltage. The error voltage polarity is inverted with respect to V_{OUT} and is therefore *-180°* out of phase with V_{OUT}. The goal of the feedback loop is to minimize the error between V_{OUT} and V_R. The error is small when the overall feedback loop gain is high. Ideally, a feedback loop would have infinite gain for all frequencies, thus providing perfect regulation regardless of the demands of the load.
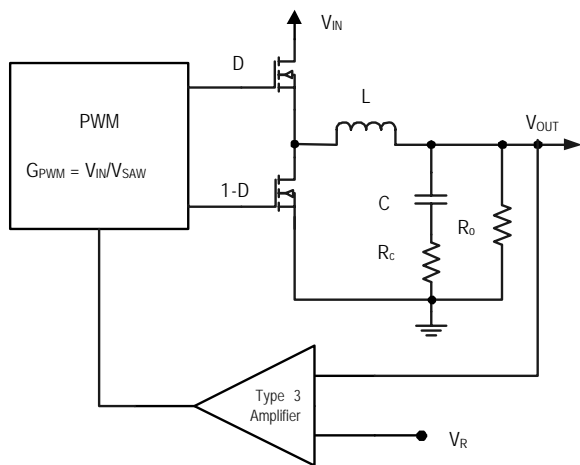

Figure 1. Simplified Buck Controller

Practical limitations such as the sampled nature of the switching power supply, finite gain and bandwidth of real components, and time delays in the control loop limit the possible gain and bandwidth of the feedback loop. In practical terms, the goal of power supply loop compensation is to have as high a gain as possible at DC and reduce this gain to less than *1* (*0dB*) before the phase shift in the control loop reaches *360°*. Recall that the error amplifier introduces *-180°* of phase shift. The output stage used in the buck converter is an LC filter. There are several characteristics of this filter that impact its frequency response. Primarily, the LC filter has *-180°* of phase shift and has an attenuation of *40dB* per decade above its natural frequency (f_n). The natural frequency of the LC filter is approximated by:

$$f_n = \frac{1}{2\pi\sqrt{LC}} \qquad \textbf{Eq. [1]}$$

Also, the components in the LC filter are not ideal because they contain parasitic impedances. In many capacitors used in output filters, the Equivalent Series Resistance (ESR, shown as R_C in Figure 1) is large enough to alter the response of the LC filter at frequencies that impact the control loop design. This is called the ESR zero (f_{zesr}). It has the effect of changing the LC filter's attenuation slope from *-40dB* (*-2* slope) per decade to *-20dB* (*-1* slope) per decade and adding *90°* of phase back into the feedback loop. The ESR zero of the output capacitor is calculated using Eq. [2]:

$$f_{zesr} = \frac{1}{2\pi C R_C} \qquad \textbf{Eq. [2]}$$

Closing the Control Loop

Frequency compensation is used to achieve the goal of less than *360°* of phase shift when the open-loop gain is above *0dB*. In the circuit of Figure 1, compensation is provided by the type 3 amplifier. The easiest method of compensating control loops using Digital-DC Technology is by using compensation pin-strap settings listed in the datasheet for each device. Zilker Labs, Inc. also offers user-friendly tools for calculating compensation coefficients using regulator design constraints and filter component parameters.

LC filters exhibit resonant behavior. Near the natural frequency (f_n), the LC filter transfer function will effectively amplify the input signal. The extent to which this occurs is determined by the quality factor (Q). In effect, the Q of the circuit is a measure of the gain the LC filter exhibits at f_n and how abrupt the phase shift from *0* to *-180°* will be. In power supply applications, it is also indirectly a measure of the circuit's efficiency: the lower the resistances in the circuit, the higher the Q. However, a high Q also corresponds to an abrupt phase shift from *0* to *-180°*.

For a simplified power stage and output filter consisting of high-side MOSFET on-resistance R_{ON-H}, low-side MOSFET on-resistance R_{ON-L}, output inductor L having resistance R_L, an output capacitance array of n parallel capacitors having capacitance C and equivalent series resistance R_C and for a load resistance R_O, the natural frequency and quality factor of the circuit are given by Equations [3] and [4], respectively.

$$f_n = \frac{1}{2\pi\sqrt{nC\left(\frac{R_C}{n}+R_O\right)\left(\frac{L}{R_e+R_O}\right)}}$$

or **Eq. [3]**

$$f_n = \frac{1}{2\pi\sqrt{LC\frac{R_C+nR_O}{R_e+R_O}}}$$

$$Q = \frac{\sqrt{nC\left(\frac{R_C}{n}+R_O\right)\left(\frac{L}{R_e+R_O}\right)}}{\frac{L}{R_e+R_O}+nC\left(\frac{R_C}{n}+\frac{R_eR_O}{R_e+R_O}\right)}$$

or **Eq. [4]**

$$Q = \frac{\sqrt{LC(R_C+nR_O)(R_e+R_O)}}{L+C(R_C(R_e+R_O)+nR_eR_O)}$$

where R_e is the effective resistance of the MOSFETs averaged over a switching period combined with the inductor resistance. For a given duty cycle, D, R_e is given by

$$R_e = D \cdot R_{ONH} + (1-D) \cdot R_{ONL} + R_L \quad \textbf{Eq. [5]}$$

For $Q > 1$, which is the case for many low-cost power supplies, the phase can be assumed to shift from *0* to *-180°* at f_n.

The PWM has a fixed gain of

$$G_{PWM} = \frac{V_{IN}}{V_{SAW}} \qquad \textbf{Eq. [6]}$$

where V_{SAW} is the peak amplitude of the PWM sawtooth waveform used in the PWM controller. G_{PWM} is a constant and has no phase impact on the feedback loop. The power stage gain, g_{PS}, (i.e., control-to-output transfer function) consists of a DC gain, G_{PS}, and a frequency-dependent component which is a function of f_{zesr}, f_n and Q.

$$g_{PS} = G_{PS}\frac{1+\dfrac{s}{2\pi f_{zesr}}}{1+\dfrac{s}{2\pi f_n Q}+\dfrac{s^2}{(2\pi f_n)^2}} \quad \textbf{Eq. [7]}$$

This transfer function is plotted in Figure 2. We define a term, G_{FIX}, which combines all the DC gains in the loop except that of the compensator.

$$G_{FIX} = G_{PWM}G_{PS} \qquad \textbf{Eq. [8]}$$

If g_{COMP} represents the gain of the compensator, the open-loop transfer function of the simplified buck converter is then

$$g = g_{COMP} G_{FIX} \frac{1 + \dfrac{s}{2\pi f_{zesr}}}{1 + \dfrac{s}{2\pi f_n Q} + \dfrac{s^2}{(2\pi f_n)^2}} \quad \textbf{Eq. [9]}$$
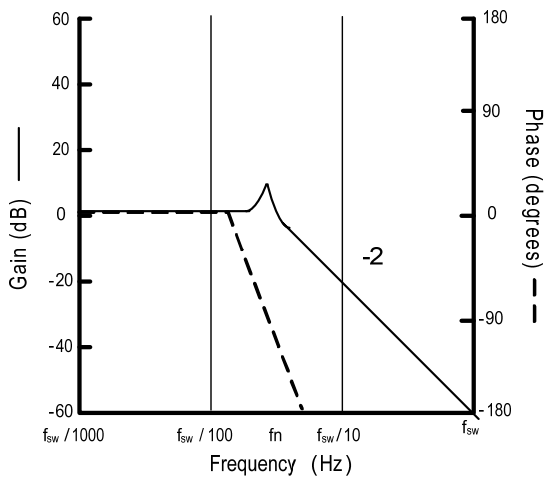
The desired feedback open-loop response is shown in Figure 3.

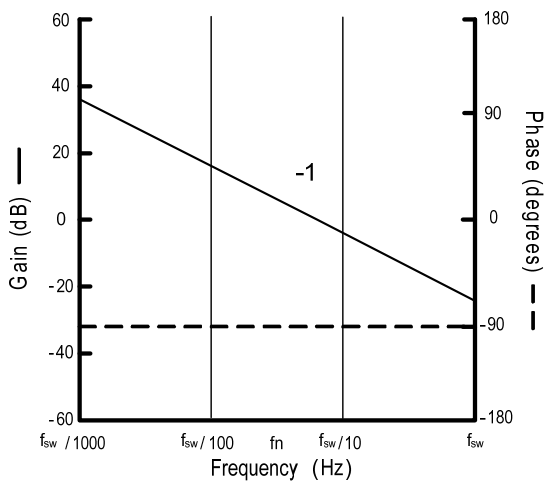**Figure 2. Buck Converter Power Stage Frequency Response**

Figure 3. Desired Open Loop Response

The goal of the compensation circuit is to modify the gain and add phase to the frequency response of the modulator and LC filter sections of the power supply (Figure 2) to achieve the desired feedback gain and

phase (Figure 3). Comparing Figure 2 and Figure 3 reveals what the frequency response of the compensation circuit should be. The compensation circuit frequency response is shown in Figure 4.
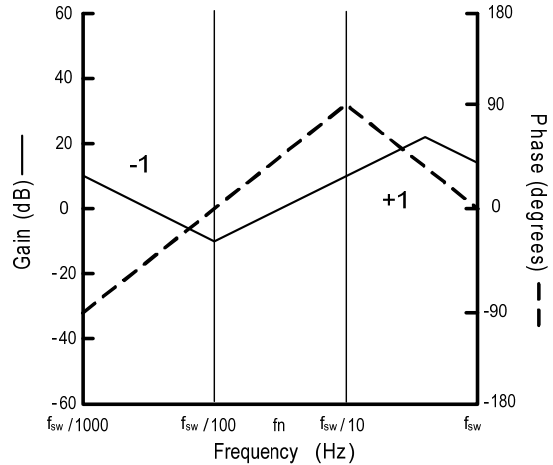

Figure 4.   Compensation Circuit Frequency Response

In a voltage mode analog power supply, this compensation is done with resistors and capacitors configured to provide poles, zeroes, and gain in the error amplifier.

To provide the highest possible gain at low frequencies, the compensator is generally chosen to be an integrator. This means that the compensator has a pole at the origin (DC), a *-1* gain slope and a phase shift of *-90°*. Because the phase shift due to the error amplifier is *-180°*, the phase shift due to the LC filter is *-180°* and the phase shift of the integrator is *-90°*, the compensator must provide a positive phase boost. In addition, because the LC filter has a *-2* gain slope and the integrator has a *-1* slope, the compensator must have a *+2* gain slope to yield the desired net gain slope of *-1*. The compensator accomplishes this with two zeroes placed near the LC filter natural frequency, f_n. These zeroes provide the *+180* phase shift and *+2* slope needed to counteract the integrator and LC filter characteristics.

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Although the loop gain is usually below *0dB* before the ESR zero, the compensator often provides a pole (*-90°*, *-1* slope) to neutralize the effects of the ESR zero (*+90°*, *+1* slope). Finally, due to limitations of real-world amplifiers, the compensator provides an additional pole to keep the error amplifier from operating beyond its gain-bandwidth product limit and to keep the switching frequency ripple from interfering with the operation of the PWM circuitry.

To complete the compensation circuit design, the amount of gain required by the compensation circuit must be determined. First, select a cross-over frequency (f_{xo}), which is a fraction of the switching frequency (f_{sw}). Generally, a ratio of *1/20* of the switching frequency is a conservative starting point (~$f_{sw}/2\pi$ is the theoretical max[1]). The gain needed from the compensator is determined by assuming the control loop is compensated so the gain plot crosses *0dB* at a *-1* slope as shown in Figure 3. The DC gain needed for this analog compensator ($G_{ACMP-DC}$) is calculated by assuming a *-1* slope for the compensated control loop for a given crossover frequency. This can be expressed as

$$G_{ACMP\_DC} = \frac{f_{xo}}{f_{sw}G_{FIX}} = \frac{1}{20G_{FIX}} \quad \textbf{Eq. [10]}$$

As noted above, the compensator has two zeroes at the LC resonant frequency (f_n). A pole is added at the ESR zero (f_{zesr}) to keep the gain of the open-loop transfer function at a slope of *-1*, and an additional pole is added at $f_{sw}/2$ to reject noise. The amplifier circuit shown in Figure 5 is used to achieve the compensation.[2]
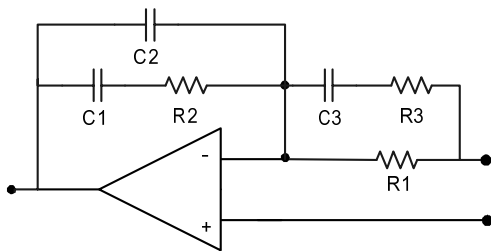

Figure 5.   Analog Compensation Amplifier

The component values are calculated using the following equations:

$$R_2 / R_1 = G_{ACMP-DC} \qquad\qquad C_1 = 1/(2\pi f_n R_2)$$
$$C_2 = 1/(2\pi f_{zesr} R_2) \qquad\qquad C_3 = 1/(2\pi f_n R_1)$$
$$R_3 = 1/(2\pi (f_{sw}/2)C_3)$$

The combination of the buck converter and compensation amplifier transfer functions yields the desired open-loop response shown in Figure 3.

Once the compensation values have been determined, the stability of the power supply can be evaluated. Using the equation for the buck converter transfer function and the gain, pole and zero locations from the compensation circuit, the resulting cross-over frequency, phase and gain margin can be evaluated. Although, ideally, the phase margin using this technique would be *90°* and the gain margin would be *20dB* or more, in reality *60°* and *6dB* are considered to be good design goals that strike a balance between performance and stability. Decreasing phase margin to less than *60°* or gain margin to less than *6dB* will increase the output voltage overshoot with transient output loads.

Digital PWM

The block diagram for a power supply controlled by a digital PWM is shown in Figure 6. The digitally controlled power supply differs from the analog version only by the values shown in the PWM block and the compensation block. The gain of the digital PWM block is seen in the functional block diagram of Figure 7.

The PWM block is derived from several functions within the device. These functions, although implemented in high speed mixed signal circuitry, can be modeled with constant values because of the relatively high frequency at which these blocks operate compared to the frequencies of interest to the control loop (i.e., *>10X* the switching frequency).
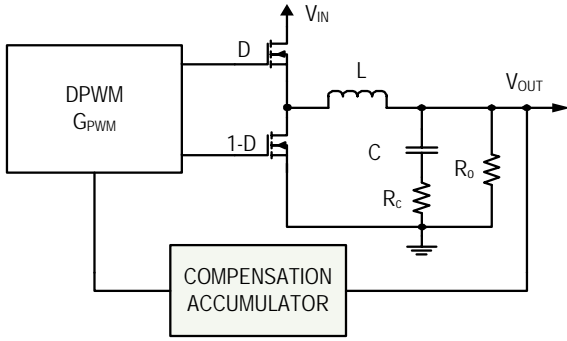
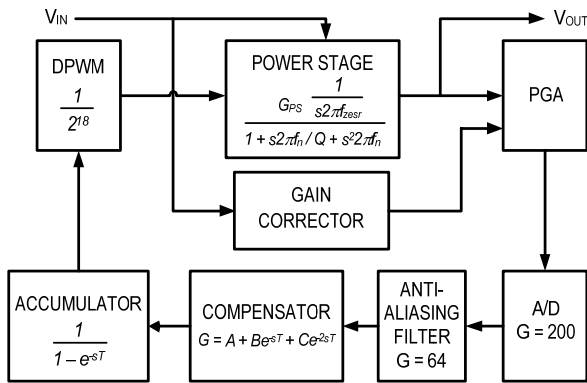**Figure 6. DPWM-Controlled Power Supply**

**Figure 7. Digital-DC Functional Block
             Diagram**

The output voltage is first applied to a programmable gain amplifier (PGA) that has a gain of between *0.2* and *2.0*. This amplifier is used to enable higher accuracy in the setting of the output voltage. Its gain is cancelled by the gain corrector, which modifies the compensation settings to yield a net gain of *1*. The gain correction function also compensates for changes in the input voltage by the same process. The gain corrector normalizes the input voltage to *5V* and automatically modifies the gain so that the net result is a loop gain that would exist if the input were at *5V*. Following the PGA, the error signal is applied to the A/D converter, which converts this error voltage into a digital value. Its gain is *1/V$_{step}$* (*1/5 mV*) or *200*. Following the A/D converter is the anti-aliasing filter, which is a multi-stage filter that provides signal gain and high frequency noise rejection. It eliminates the need for the second pole used in the analog compensator. As can be seen in Figure 8, it has a fixed

gain of *64* at low frequencies, but a large attenuation at the switching frequency without adding excessive phase loss. This phase loss can be expressed as a function of the switching frequency and is discussed later as part of the compensation.
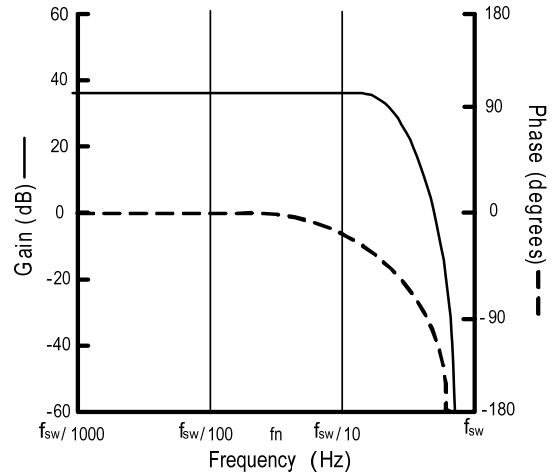

Figure 8. Anti-Aliasing Filter Response

After passing through the compensator and accumulator, the signal is applied to the digital pulse width modulator (DPWM). The DPWM converts the output of the integrator into the duty cycle that is applied to the power supply MOSFETs. In summary, the DPWM block in Figure 6 is a combination of the PGA, the gain of the A/D, the anti-aliasing filter, and the DPWM. This is also a fixed gain and can be expressed as

$$G_{FIX} = \frac{5 \cdot 200 \cdot 64}{2^{18}} G_{PS} \qquad \textbf{Eq. [11]}$$

The transfer function of the digital voltage mode converter can now be expressed as an equation in the same form as the analog controller:

$$g = g_{COMP} G_{FIX} \frac{1 + \dfrac{s}{2\pi f_{zesr}}}{1 + \dfrac{s}{2\pi f_n Q} + \dfrac{s^2}{(2\pi f_n)^2}} \textbf{ Eq. [12]}$$

As mentioned earlier, the analog compensator of Figure 5 provides two zeroes to cancel the two poles of Equation [12] (at f_n), but it also provides three poles. One of these poles cancels the ESR zero of Equation [12] (at f_{zesr}), a high frequency pole (at $f_{sw}/2$) improves noise immunity and the third pole is at the origin – an integrator which provides the desired response of a slope of -1. Finally, the analog compensator provides a DC gain term ($G_{ACMP-DC}$) which ultimately determines the crossover frequency and impacts phase margin and gain margin as well. To obtain the ideal response of Figure 3 and provide noise rejection above $f_{sw}/2$, the analog compensator's transfer function must be

$$g_{ACMP} = G_{ACMP\_DC} \frac{\left(1 + \frac{s}{2\pi f_n Q} + \frac{s^2}{(2\pi f_n)^2}\right)}{s\left(1 + \frac{s}{2\pi f_{zesr}}\right)\left(1 + \frac{s}{\pi f_{sw}}\right)} \quad \textbf{Eq. [13]}$$

Transforming Equation [12] to the digital domain yields an equation of the form

$$g_Z = g_{ZCOMP} G_{ZFIX} \frac{\left(1 - dz^{-1}\right)}{\left(1 - bz^{-1} + cz^{-2}\right)} \quad \textbf{Eq. [14]}$$

where g_{ZCOMP} is the z-domain compensator, G_{ZFIX} is a transcendental function of G_{FIX}, f_n, f_{zesr} and f_{sw} representing the DC gain in the z-domain, d is a transcendental function of f_{zesr} and f_{sw}, and b and c are transcendental functions of f_n and f_{sw}. It should be noted that, for $Q > 0.5$, b becomes complex but may be converted to a real number using Euler's identity.

The digital control loop is compensated in much the same way as the analog control loop. However, because the digital control loop has an anti-aliasing filter that provides noise rejection above $f_{sw}/10$, the poles at f_{zesr} and $f_{sw}/2$ in Eq. [13] are not required in the digital compensation filter. For this reason, the crossover frequency should occur at least one octave before the ESR zero ($f_{xo} \leq f_{zesr}/2$). The pole at the origin is implemented using an accumulator. Again, a crossover frequency of $f_{xo} = f_{sw}/20$ is selected and the DC gain of the digital compensator is calculated, using an equation similar to Equation [10] for the analog compensator:

$$G_{ZCMP\_DC} = \frac{f_{xo}}{f_{sw} G_{ZFIX}} = \frac{1}{20 \cdot G_{ZFIX}} \quad \textbf{Eq. [15]}$$

Like the analog compensator, the digital compensator has two zeroes at the LC resonant frequency (f_n). Instead of an op-amp circuit, the digital compensator uses a recursive filter, which is simply an adder with four inputs: 1) the output of the A/D converter (the error voltage) multiplied by a constant, 2) the error voltage from the previous switching cycle (shown as z^{-1}) multiplied by another constant, 3) the integrator and 4) the error voltage from the switching cycle two cycles previous (shown as an additional z^{-1}) multiplied by a third constant. This filter is shown schematically in Figure 9.
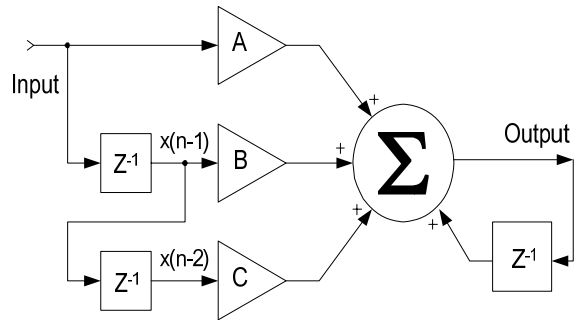

Figure 9. Digital Compensator / Recursive Filter

By substituting $z^{-1} = e^{-sT}$ for each delay (where T is the sampling period), the digital compensator / recursive filter can be represented as follows:

$$g_{ZCOMP} = \frac{A + Bz^{-1} + Cz^{-2}}{\left(1 - z^{-1}\right)}$$

or **Eq. [16]**

$$g_{COMP} = \frac{A + Be^{-sT} + Ce^{-2sT}}{\left(1 - e^{-sT}\right)}$$

The term $1/(1 - e^{-sT})$ is due to the accumulator and models both the gain and phase response of the integrator. Although in transcendental form, the digital compensator / recursive filter can be configured to have the same response as the analog compensator by selecting appropriate constants for A, B and C in Eq. [16].

To do so, set like terms equal in the numerator of Eq. [16] and the denominator of Eq. [14], being sure to divide by the compensator DC gain, $G_{ZCMP\text{-}DC}$. This yields Equations [17] for real zeroes (at f_{z1} and f_{z2}) and Equations [18] for complex zeroes (at f_n for $Q > 0.5$). To simplify these equations, new terms r_1 and r_2 are defined for Eq. [17] and r and θ are defined for Eq. [18].

Compensation Coefficients for Real Zeroes:

$$Let \quad r_1 \equiv e^{\frac{-2\cdot\pi\cdot f_{z1}}{f_{sw}}} \quad r_2 \equiv e^{\frac{-2\cdot\pi\cdot f_{z2}}{f_{sw}}}$$

$$A = \frac{G_{ZCMP-DC}}{(1-r_1)\cdot(1-r_2)}$$

Eq. [17]

$$B = -A\cdot(r_1+r_2)$$

$$C = A\cdot r_1 \cdot r_2$$

Compensation Coefficients for Complex Zeroes:

$$Let \quad r \equiv e^{\frac{-\pi\cdot f_n}{Q\cdot f_{sw}}} \quad \theta \equiv \frac{2\pi f_n}{f_{sw}}\cdot\sqrt{1-\frac{1}{4\cdot Q^2}}$$

$$A = \frac{G_{ZCMP-DC}}{1-2\cdot r\cdot\cos\theta + r^2}$$

Eq. [18]

$$B = -A\cdot 2\cdot r\cdot\cos\theta$$

$$C = A\cdot r^2$$

As with the analog compensator, select the zero frequencies and the gain desired for the compensator stage. Solve the equations to yield the appropriate *A*, *B*, and *C* coefficients. These coefficients are loaded into the digital compensator using a PMBus command. Additional details on the use of the PMBus for loading compensation coefficients are in Application Note AN2013.[3] The power supply response can be simulated and tested in the same manner as an analog controller.

The digital compensator also provides a means of correcting for the *Q* of the LC filter. Using the calculated coefficients, both the gain and phase of the LC filter are cancelled by the digital compensator, as shown in Figure 10.
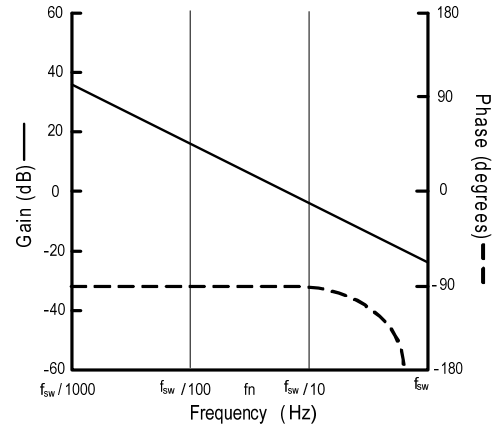

Figure 10. Open-Loop Response

As mentioned previously, Zilker Labs, Inc. offers user-friendly tools for calculating compensation coefficients using regulator design constraints and filter component parameters. Contact your regional sales office for details.

Performance Verification

Once the coefficients have been loaded into the device, the circuit can be tested for stability and transient response performance. Transient response is the easiest to test. It is done by applying a rapidly changing output current, or step load, to the output and measuring the response using an oscilloscope. If a programmable electronic load is available,

• Set the step load slew rate to that of the expected end-use application.

• Set the load step to cause a *1-3%* deviation in the output voltage.

• Set the step duty cycle to ~*50%*

• Select a repetition frequency that allows the power supply to settle after each transition; $f_{xo}/100$ should be a good starting point.

The power supply output should be 95% settled within three time-constants of the crossover frequency, or

$$t_{95\%} \approx 3\cdot\tau_{xo} = \frac{3}{2\pi f_{xo}}$$

Eq. [19]

The response to the step load may have some overshoot. However, more than three oscillations indicate marginal stability; an exponential decay is preferred.

The control-loop response should also be verified by injecting a frequency swept signal into the loop and measuring the frequency response with a network analyzer. This is done by placing a small resistor (*10 – 100Ω*) between the output and the VSEN pin and injecting the signal into the feedback loop by applying a floating AC signal across this resistor, as shown in Figure 11. The voltage from VSEN to ground is the input signal (sometimes called reference signal), and the power supply output voltage (*V_OUT*) is the output signal (sometimes called the test signal). The network analyzer will read out the relative phase and gain of the transfer function: output signal/input signal. The goal is to verify a phase margin of *>60°* and a gain margin of *>6dB* over a range of operating conditions. The test signal should be monitored with an oscilloscope and adjusted so that the test signal peak amplitude does not exceed *1%* of the *V_OUT*. Excessive test signal amplitude will result in erroneous loop gain measurements. Proper correlation between measurements and simulations depends on the accuracy of the models used, and Zilker Labs, Inc. is constantly working to ensure the accuracy of its models.
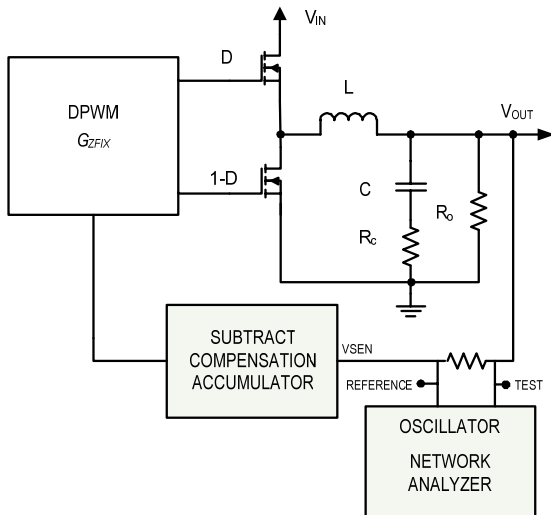
References

[1]   Lloyd H. Dixon, Jr., *Control Loop Cookbook*, Unitrode Power Supply Design Seminar Manual SEM-1100, 1996, p. 5-20.

[2]   Venable, Dean and Foster, S. R., *Practical Techniques for Analyzing, Measuring and Stabilizing Feedback Control Loops in Switching Regulators and Converters*, PowerCon7 Proceedings, 1980.

[3]   AN2013 – *Zilker Labs PMBus™ Command Set*, Zilker Labs, 2006.

Revision History

Date	Rev. #	
09/27/2006	1.0	Initial Release
10/12/2006	1.1	Update Eqs 5, 8 and 14
06/14/2007	1.2	Corrected Fig 11.
09/04/2007	1.3	General updates.
09/04/2007	1.31	Minor text revisions.
12/06/2007	1.32	Corrected loop response descriptions to say "open loop"
05/01/2009	AN2016.0	Assigned file number AN2016 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to application note content.

Figure 11. Loop Gain Measurement

NOTES

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